

FIG. 1

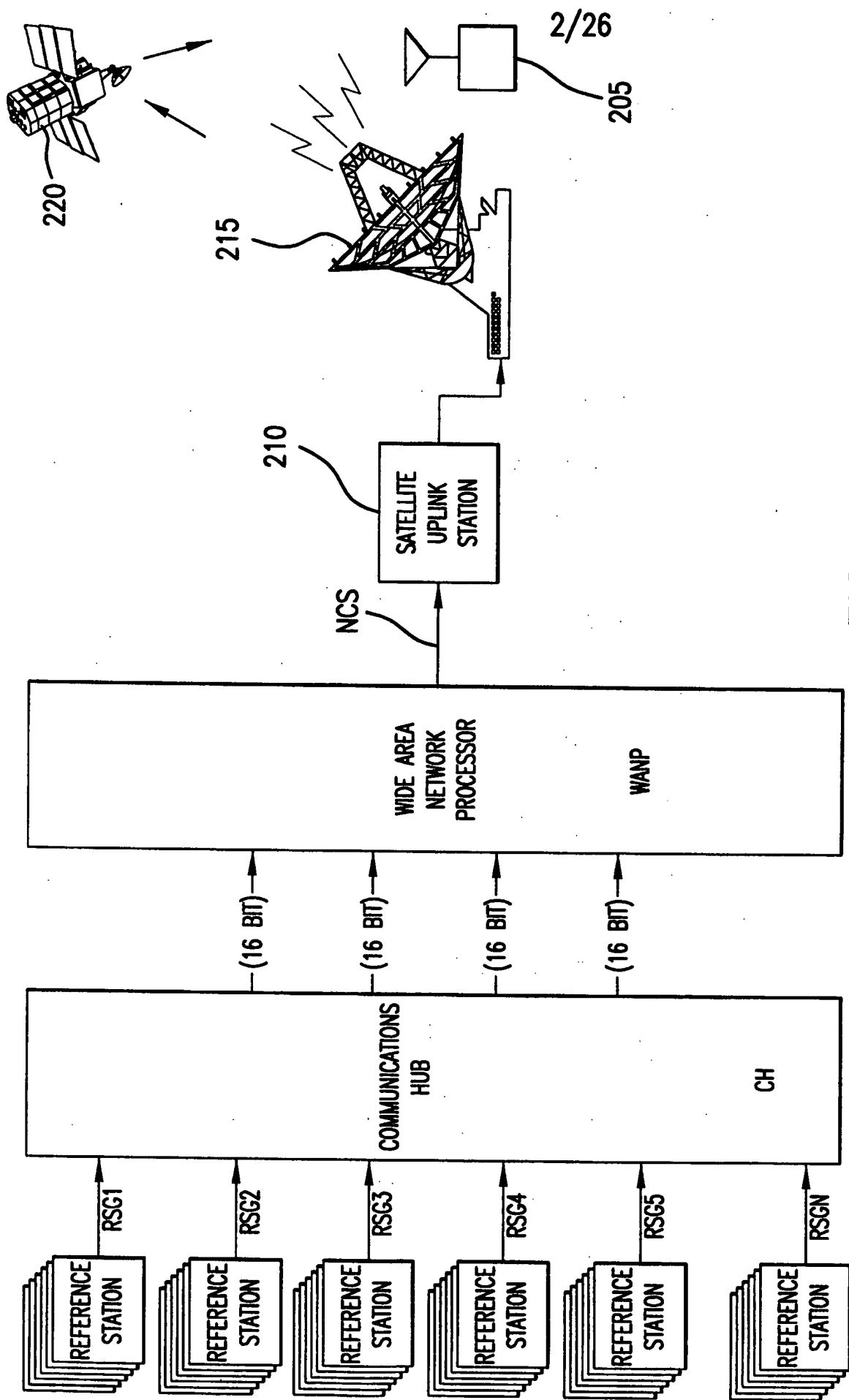


FIG. 2

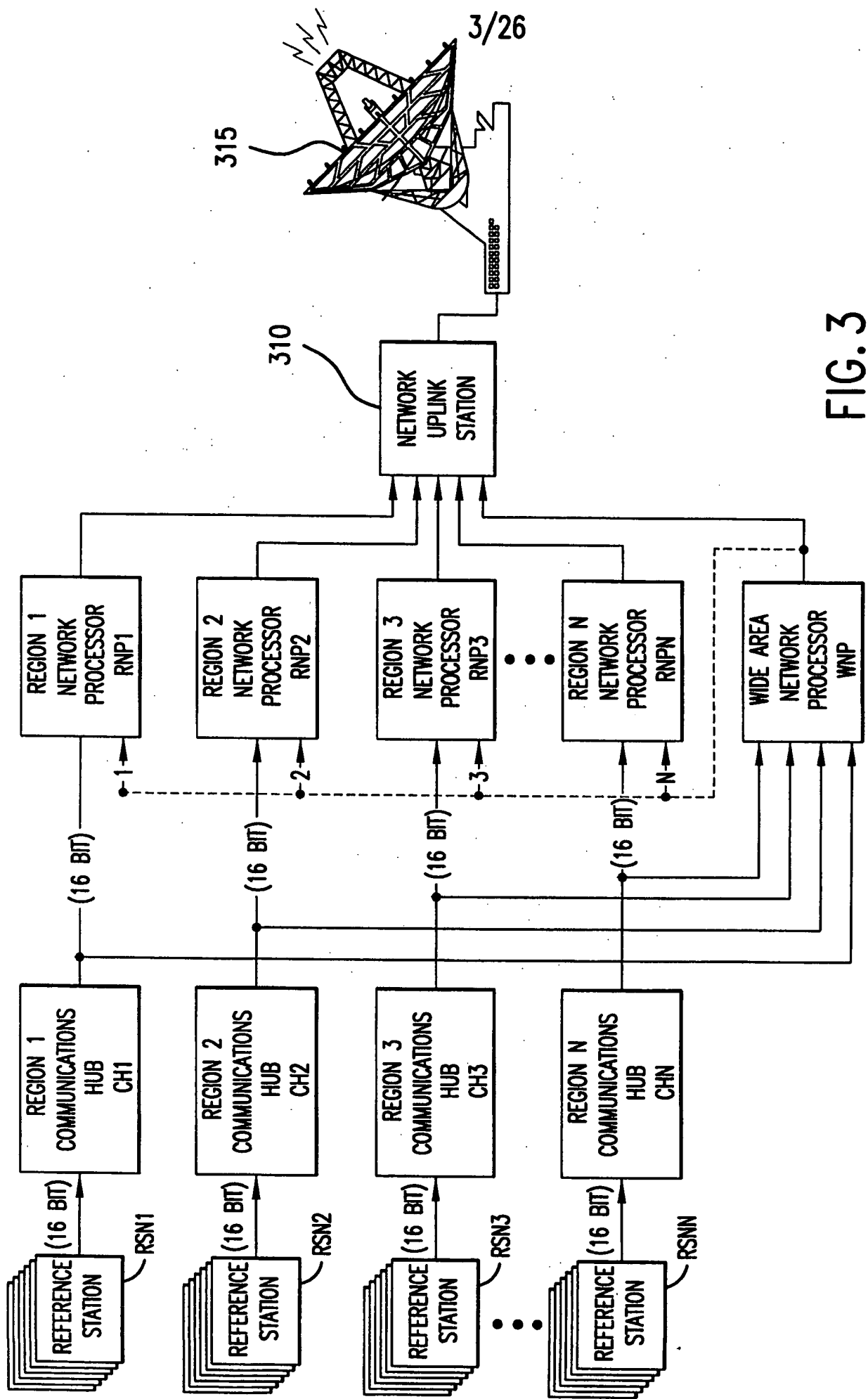


FIG. 3

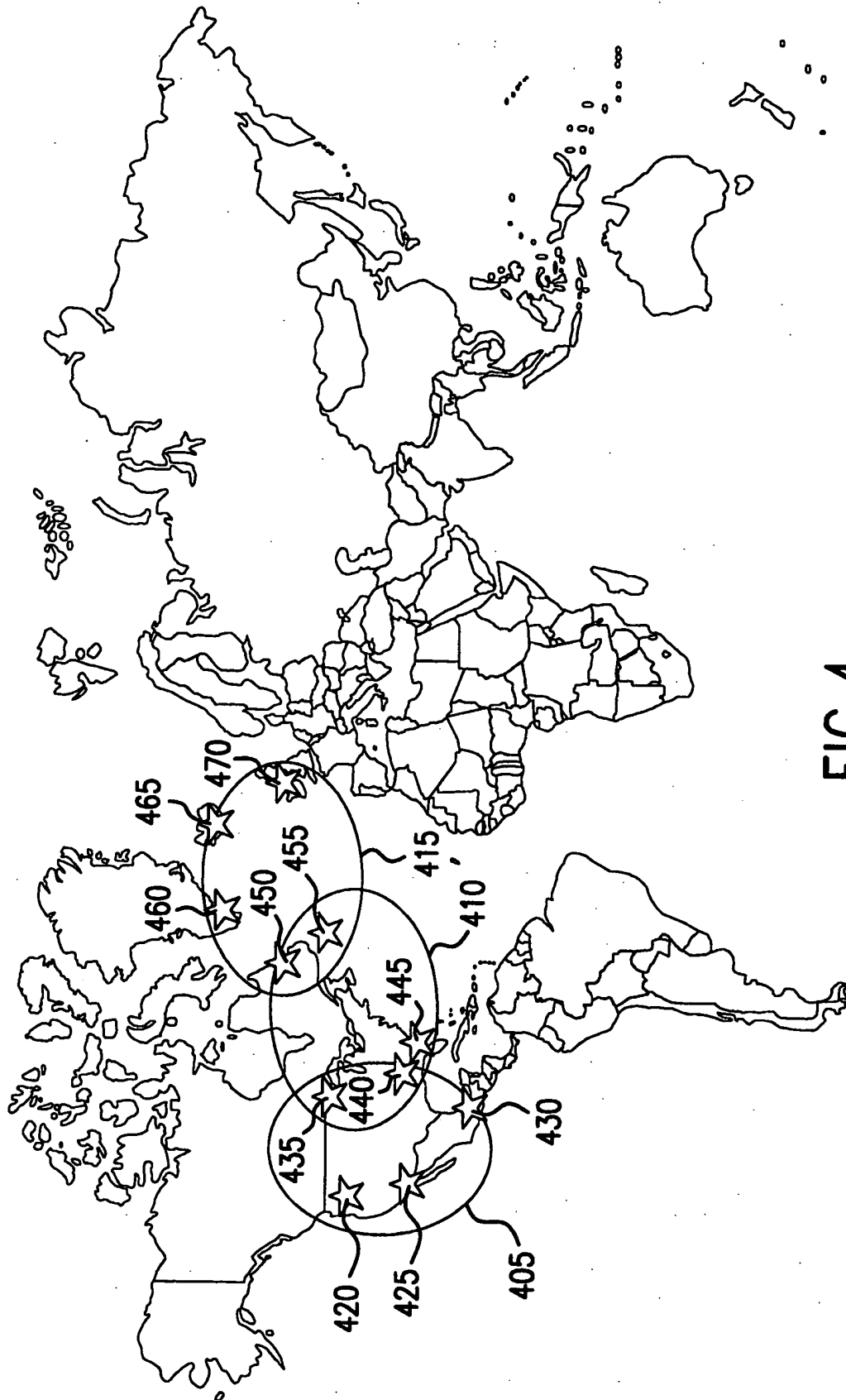
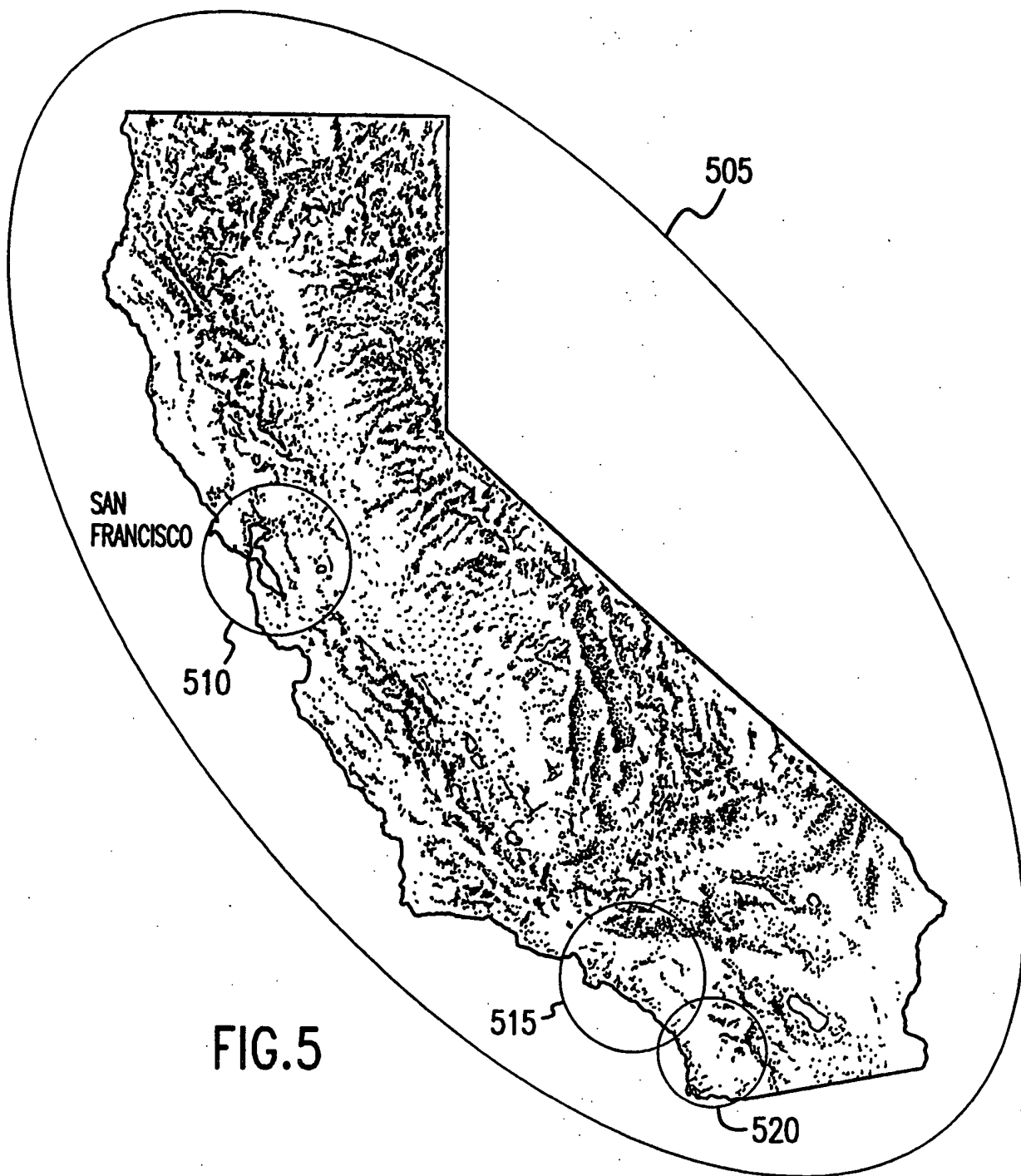


FIG.4



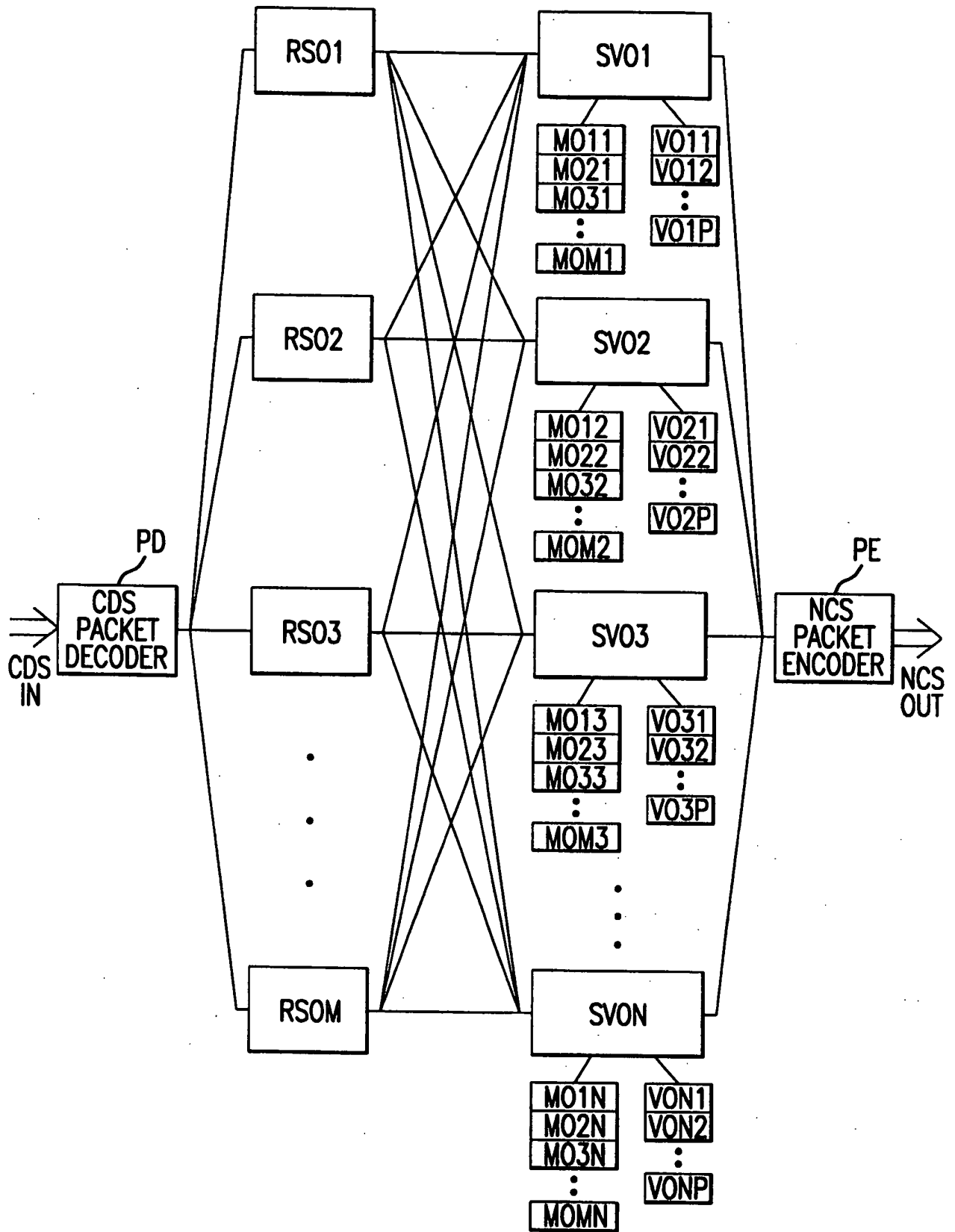


FIG. 7

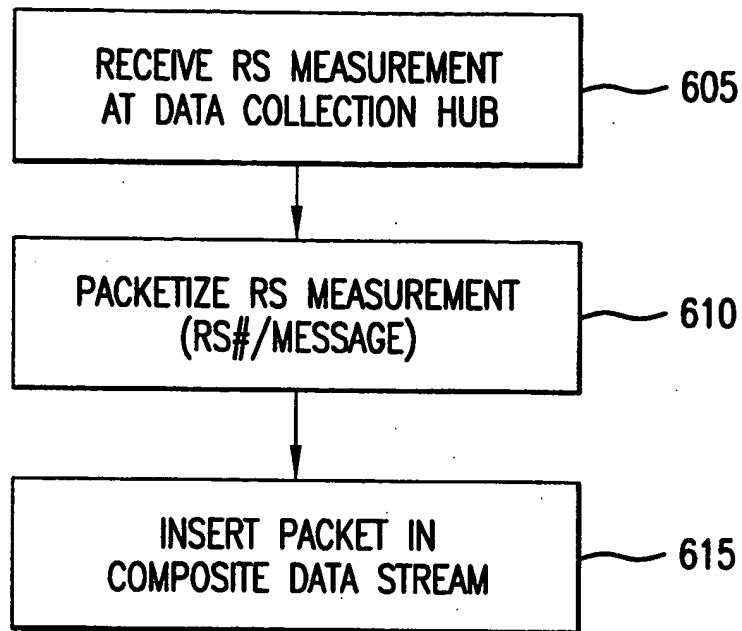
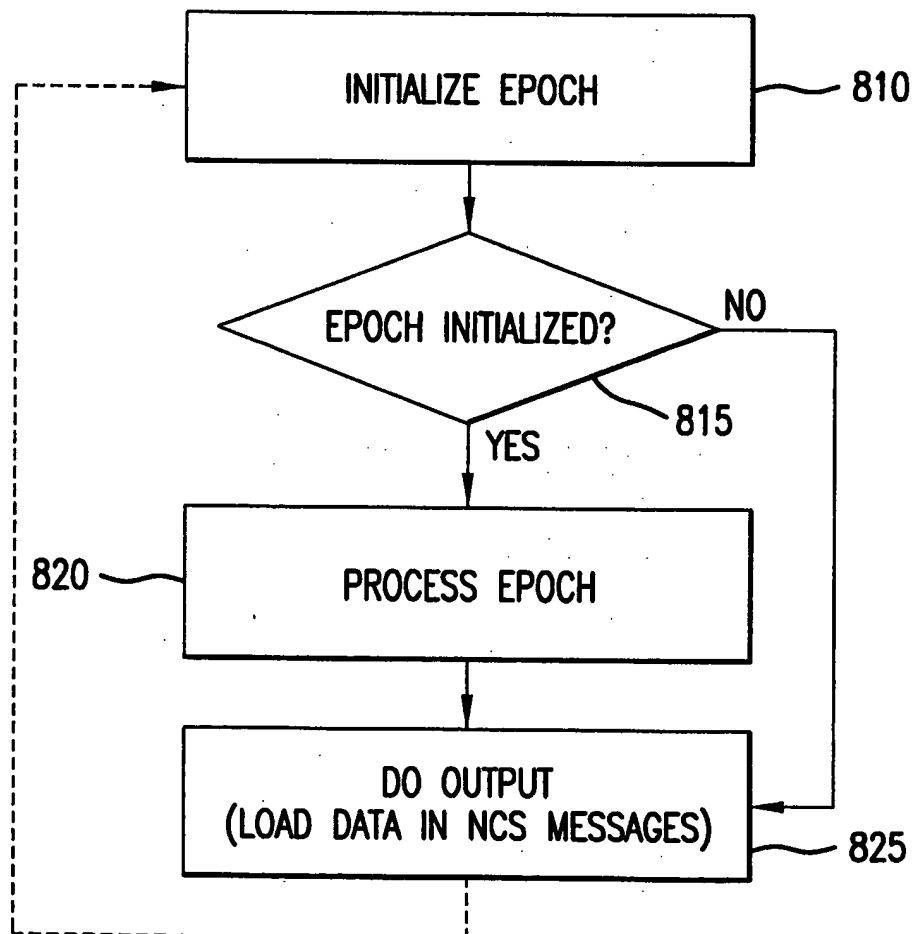
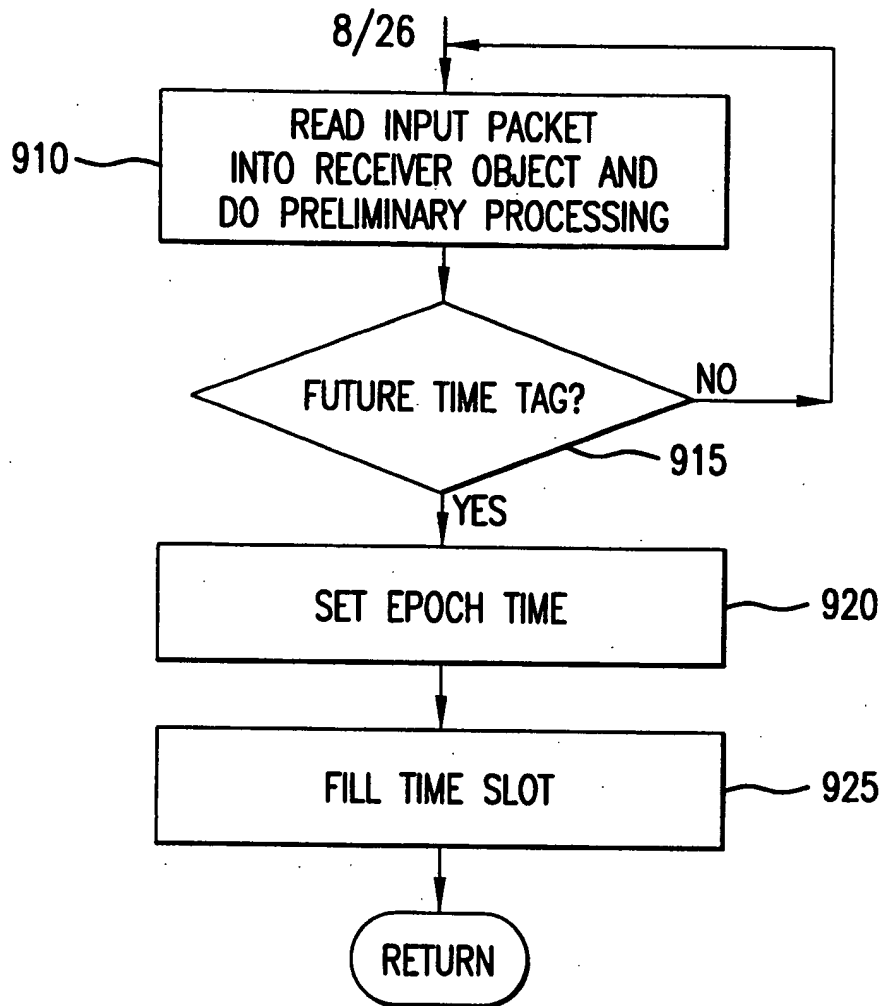


FIG. 6



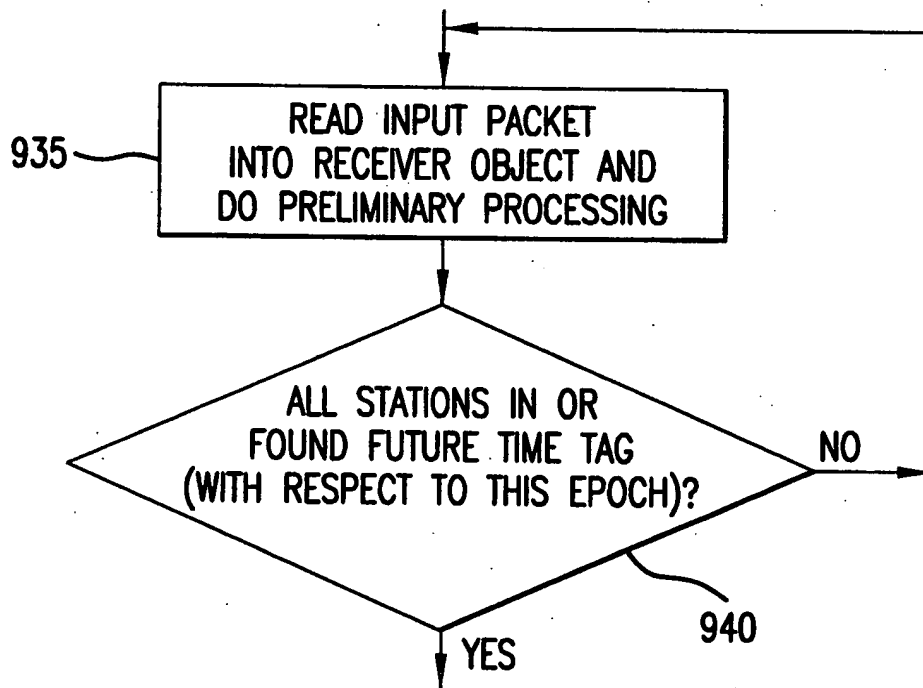
NETWORK PROCESSOR FLOW

FIG. 8



INITIALIZE EPOCH 810

FIG. 9A



FILL TIME SLOT 925

FIG. 9B



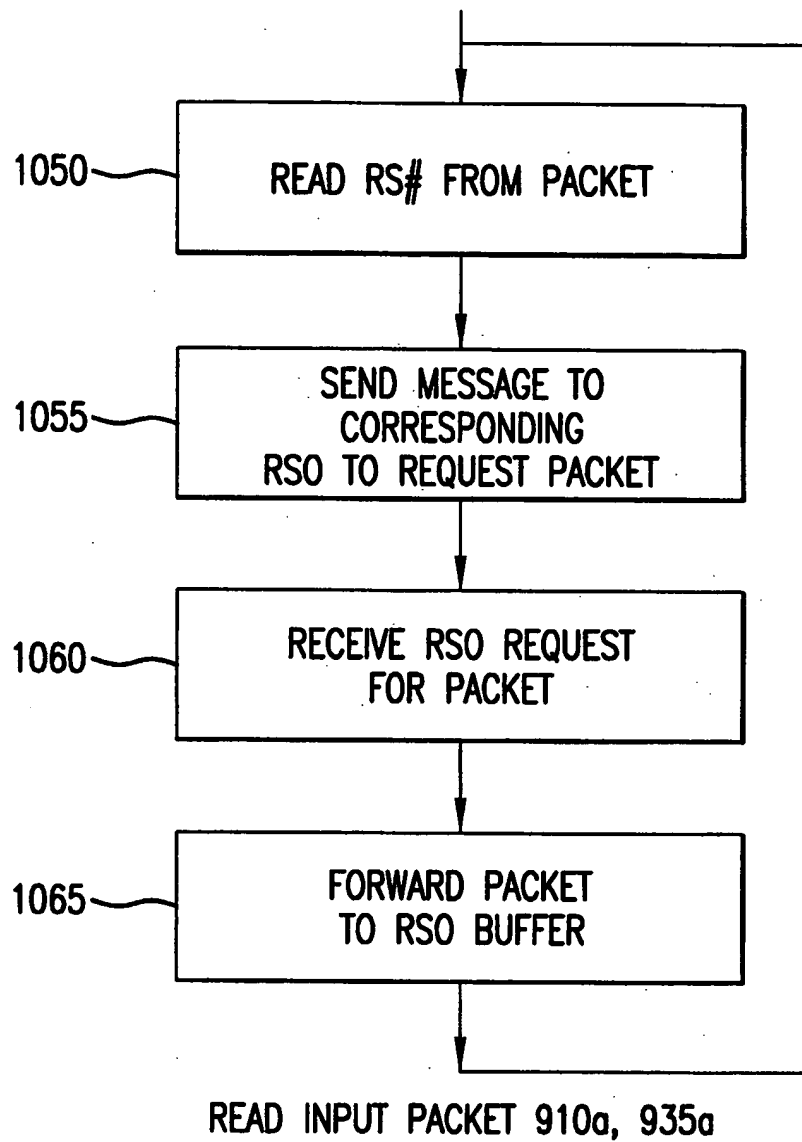
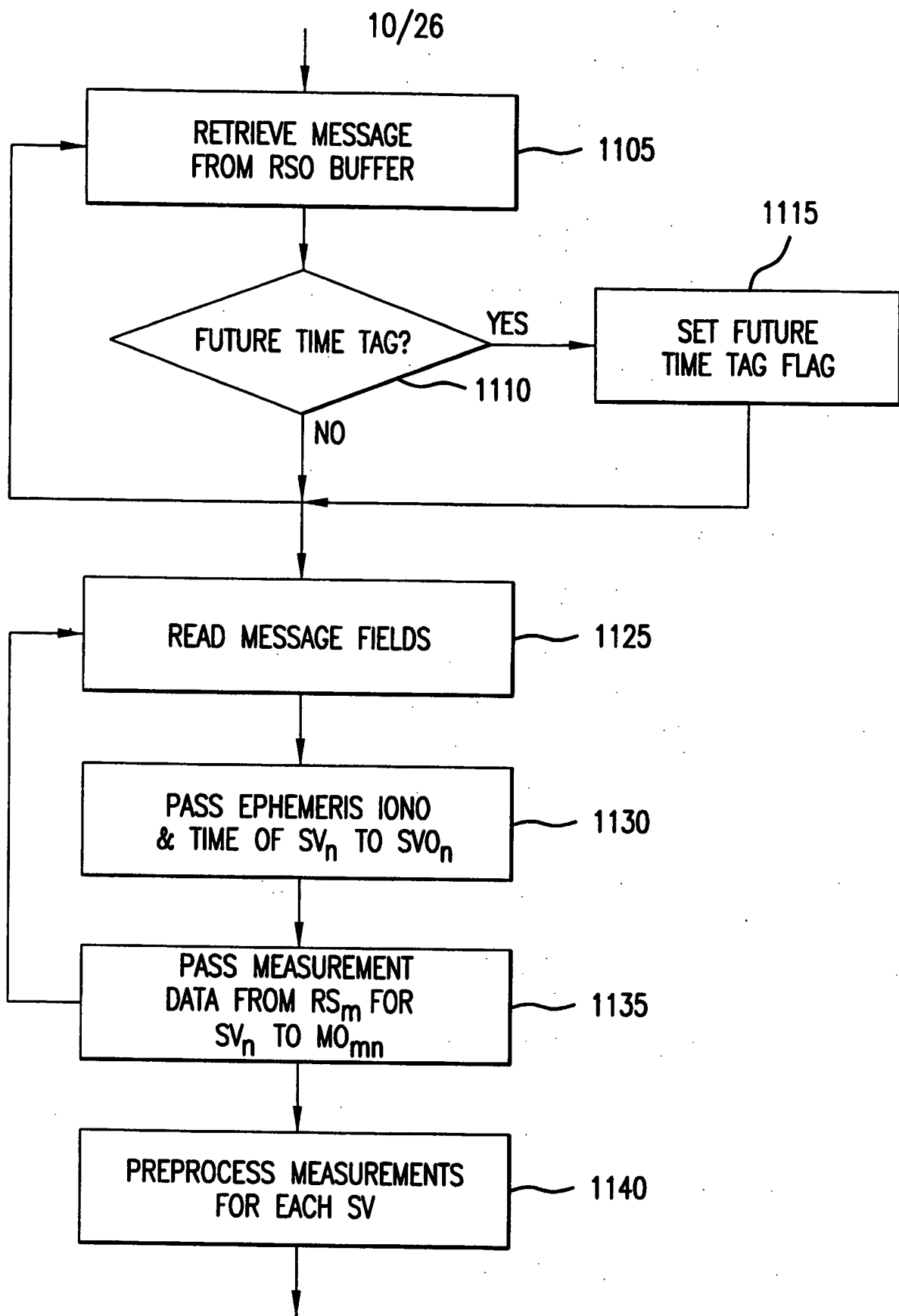
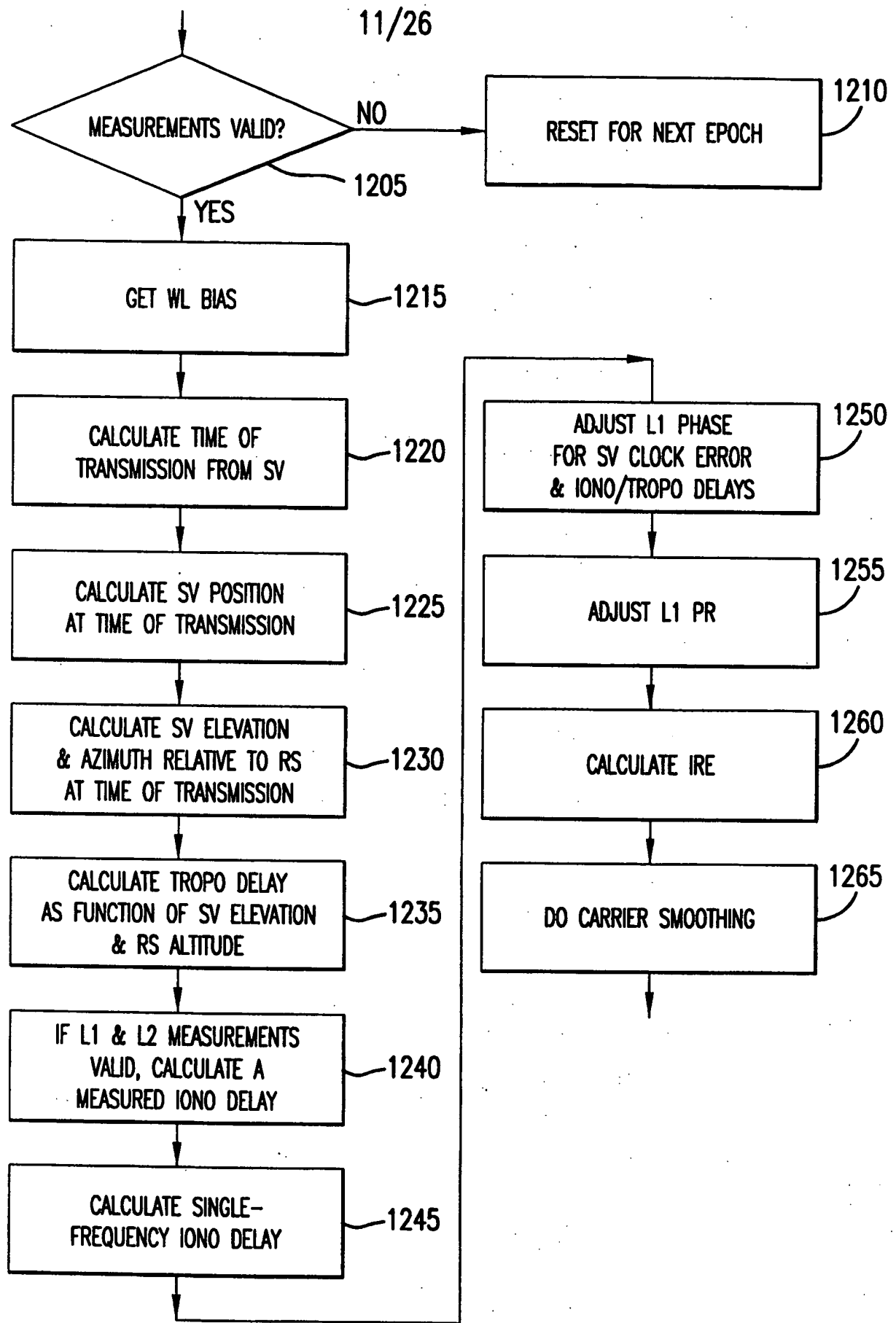


FIG. 10



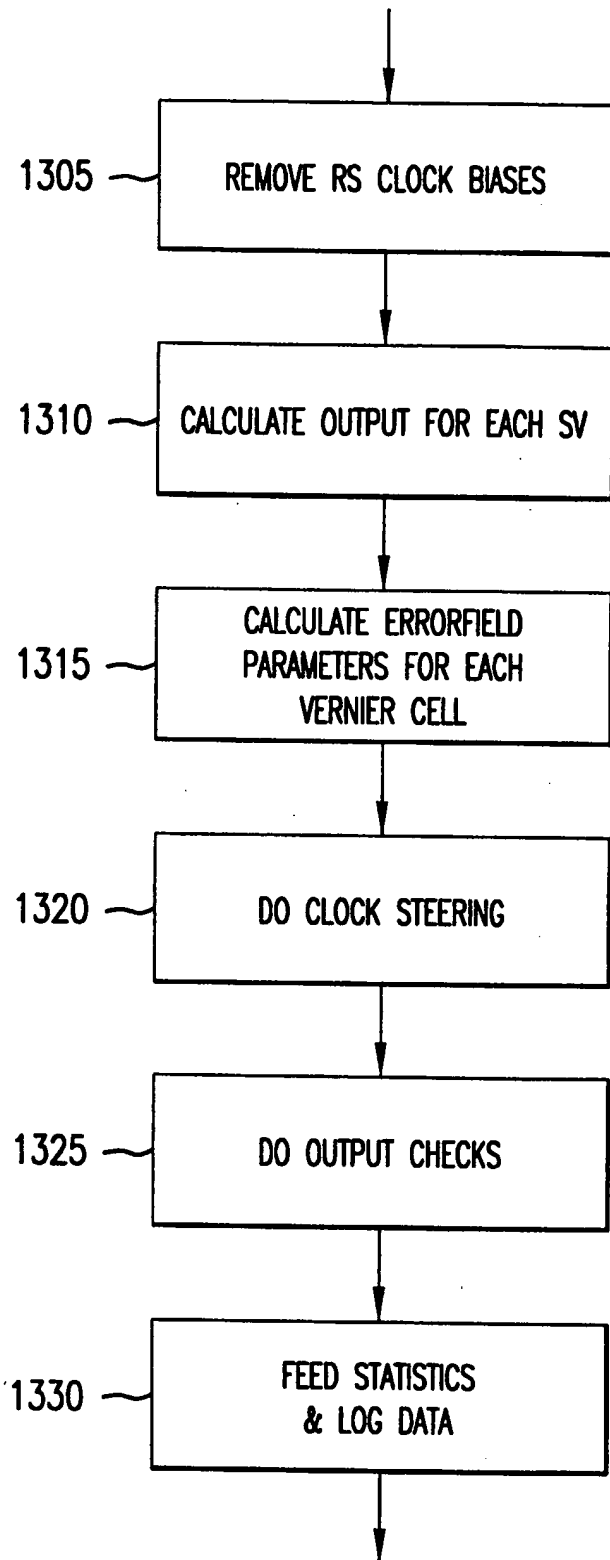
READ INPUT PACKET 910b, 935b

FIG. 11

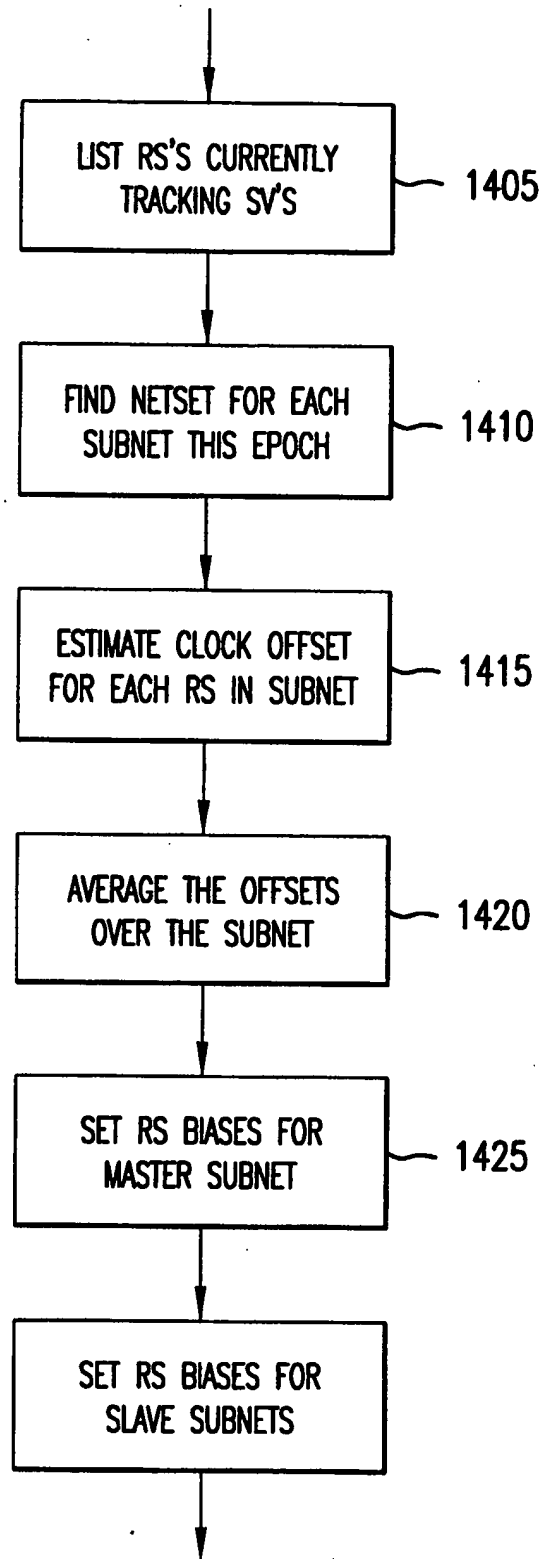


PREPROCESS MEASUREMENTS 1140

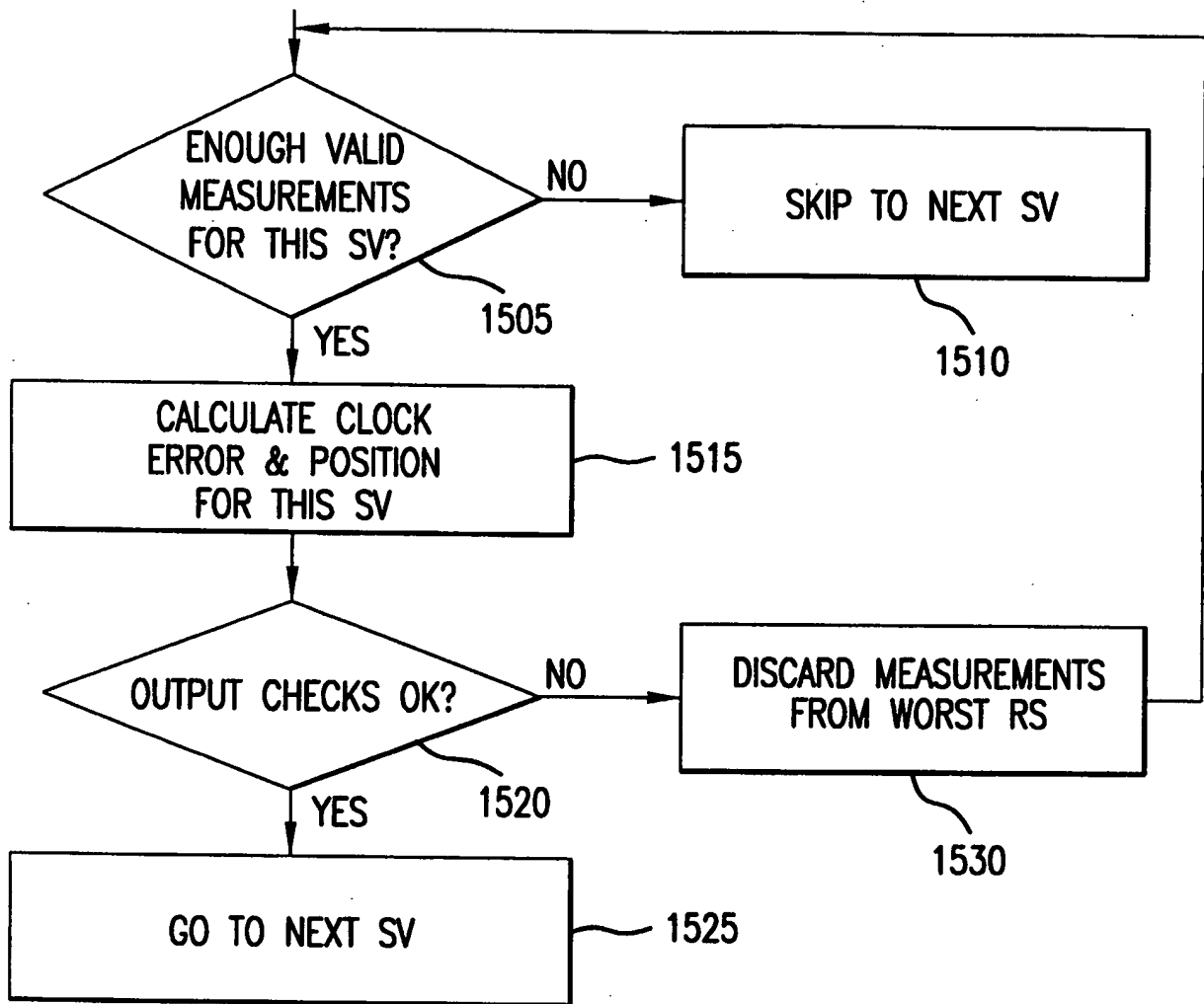
FIG. 12



PROCESS EPOCH 920  
FIG. 13

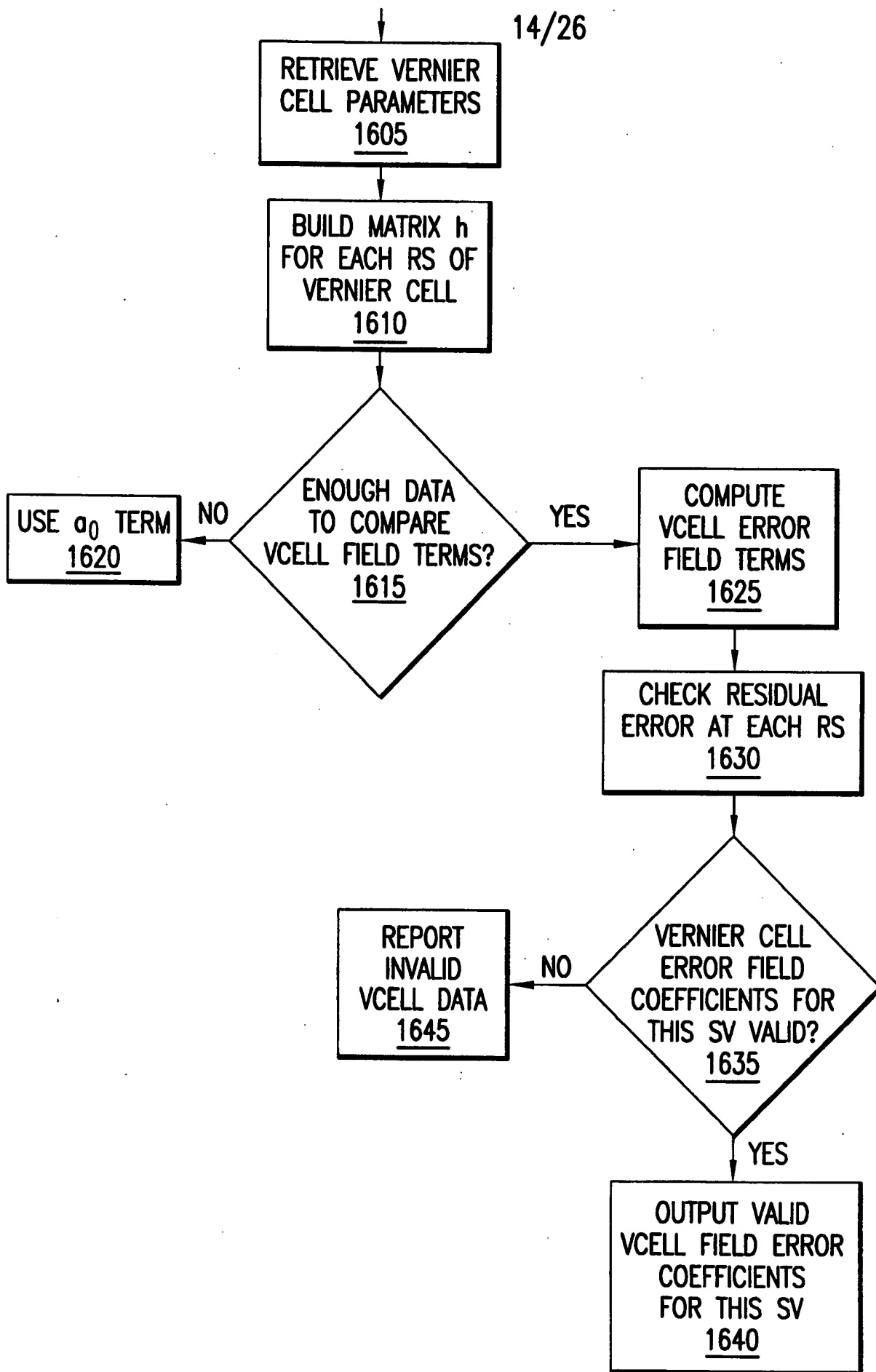


REMOVE RS CLOCK BIASES 1305  
FIG. 14



CALCULATE OUTPUT FOR EACH SV 1310

FIG. 15



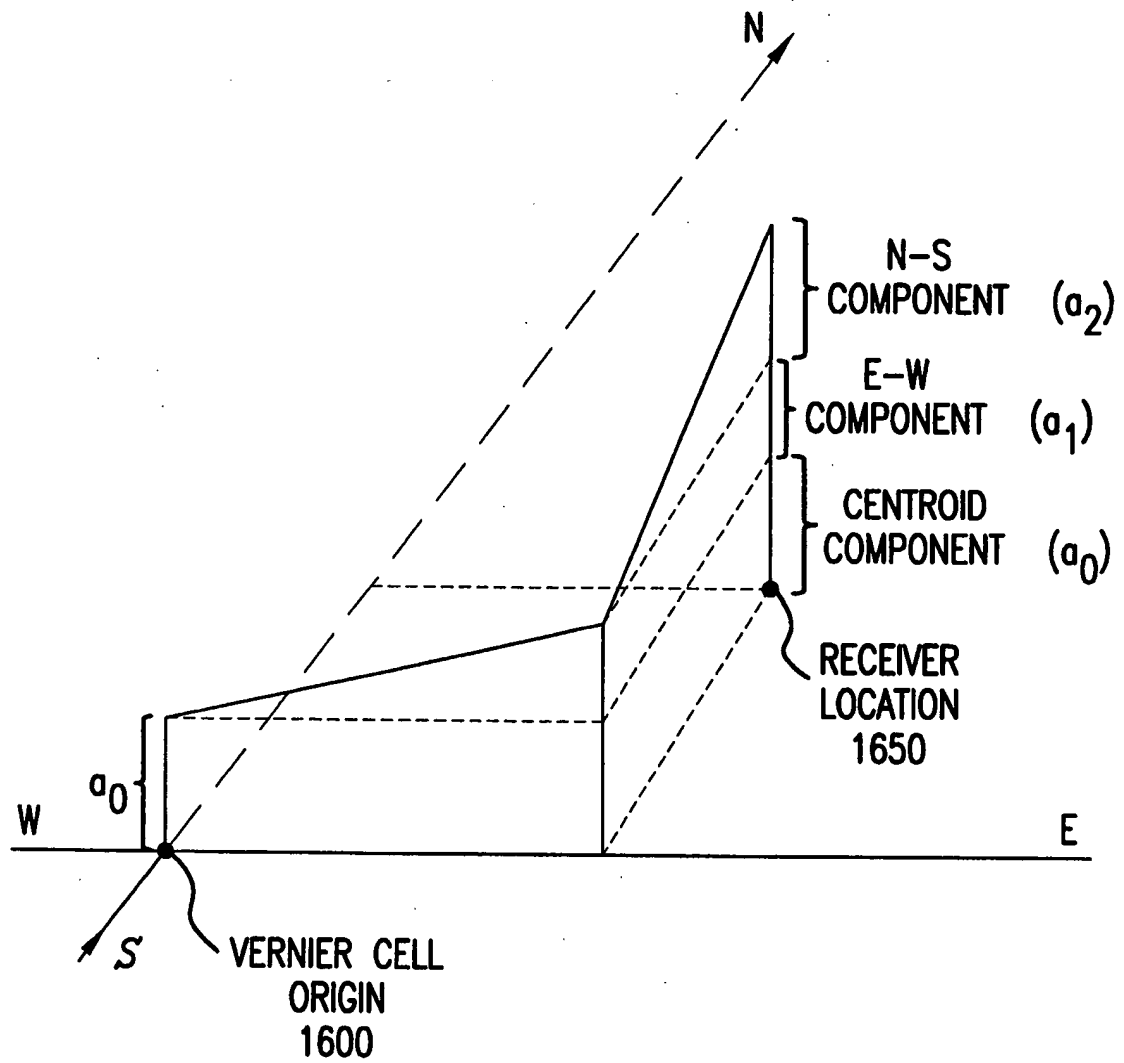


FIG. 16B

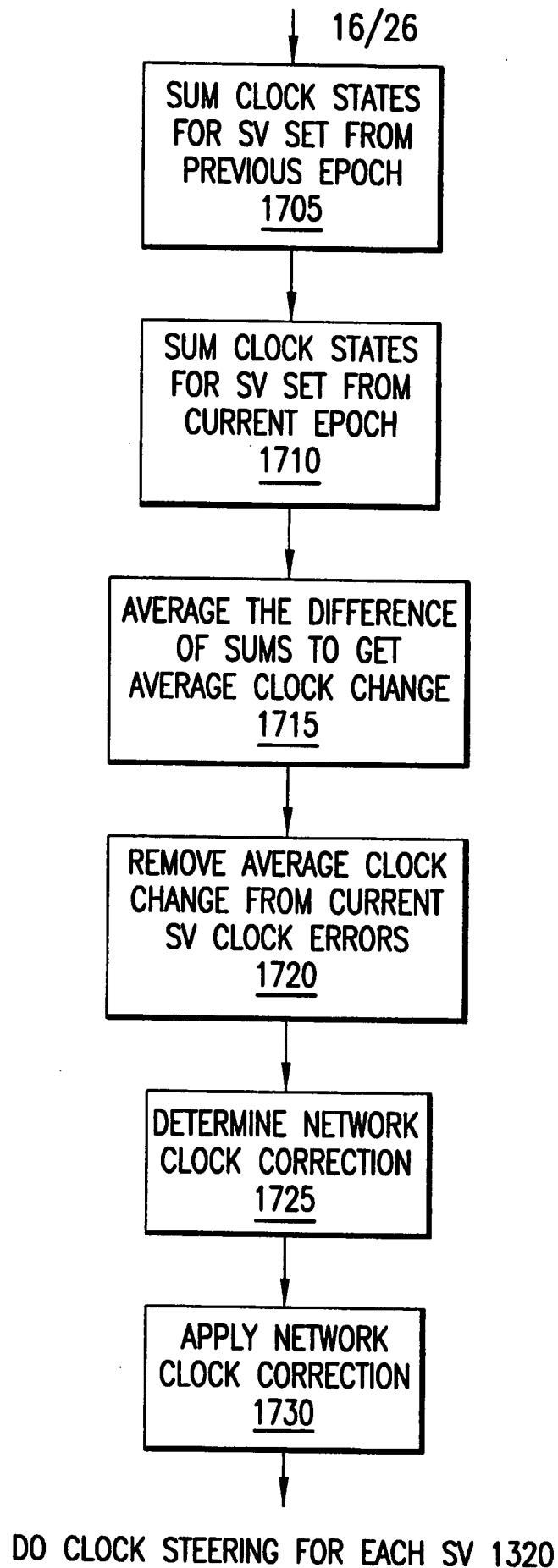


FIG. 17



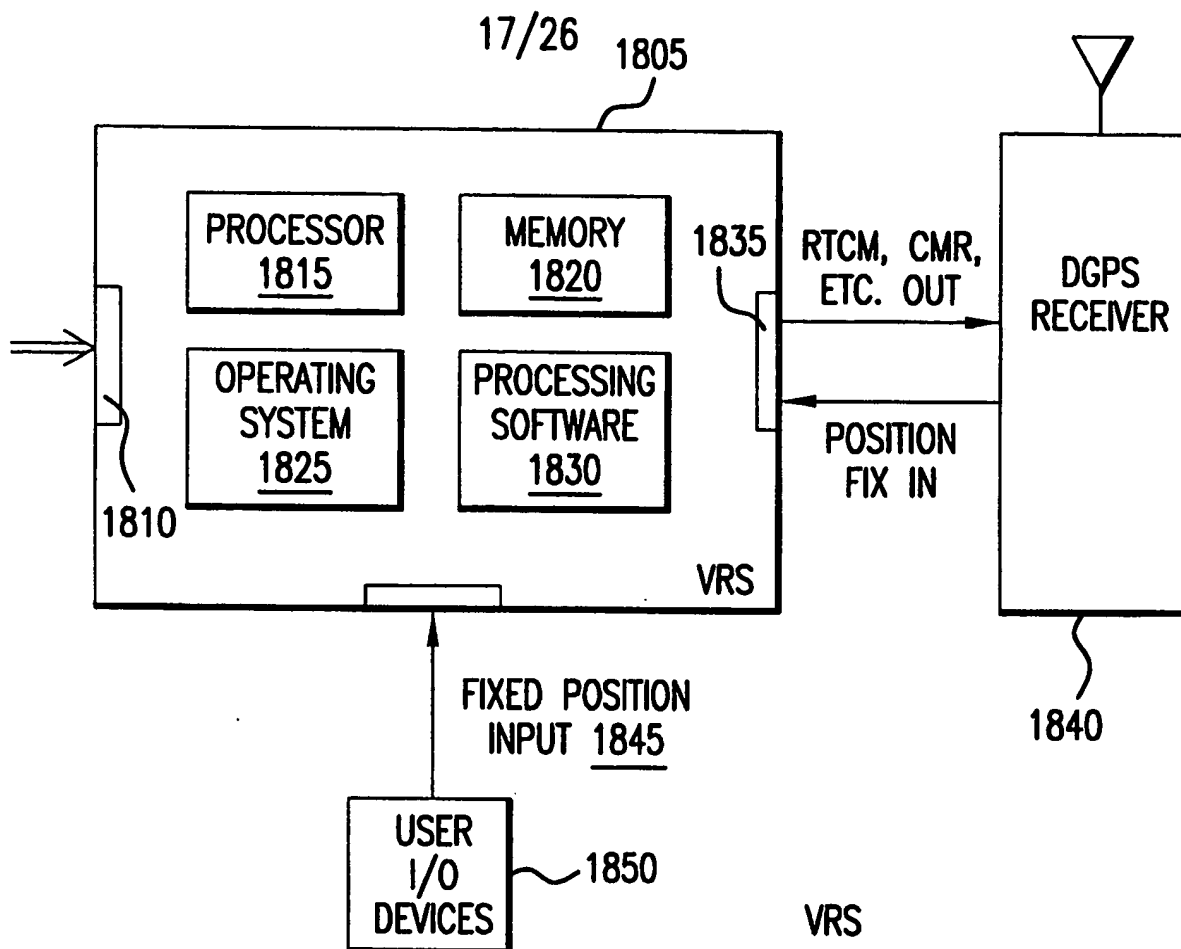


FIG. 18

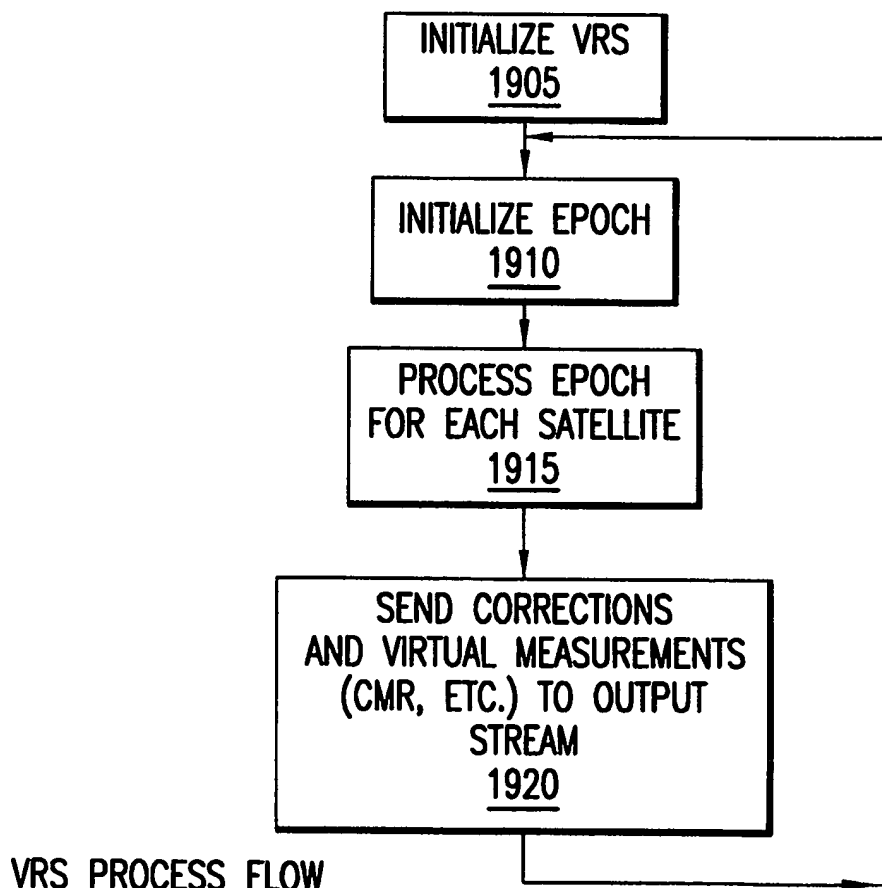


FIG. 19

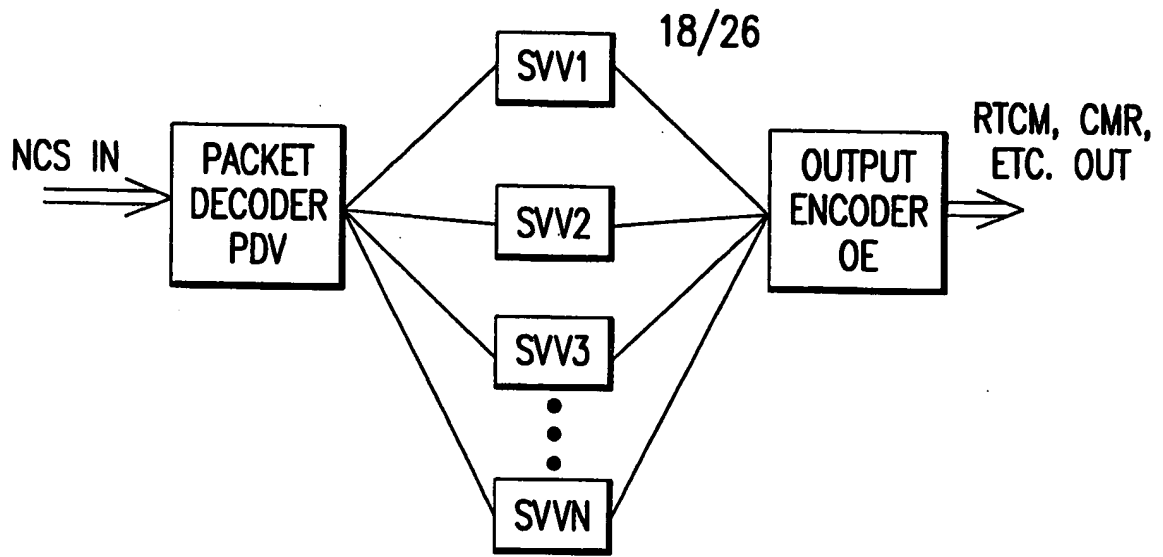


FIG. 20

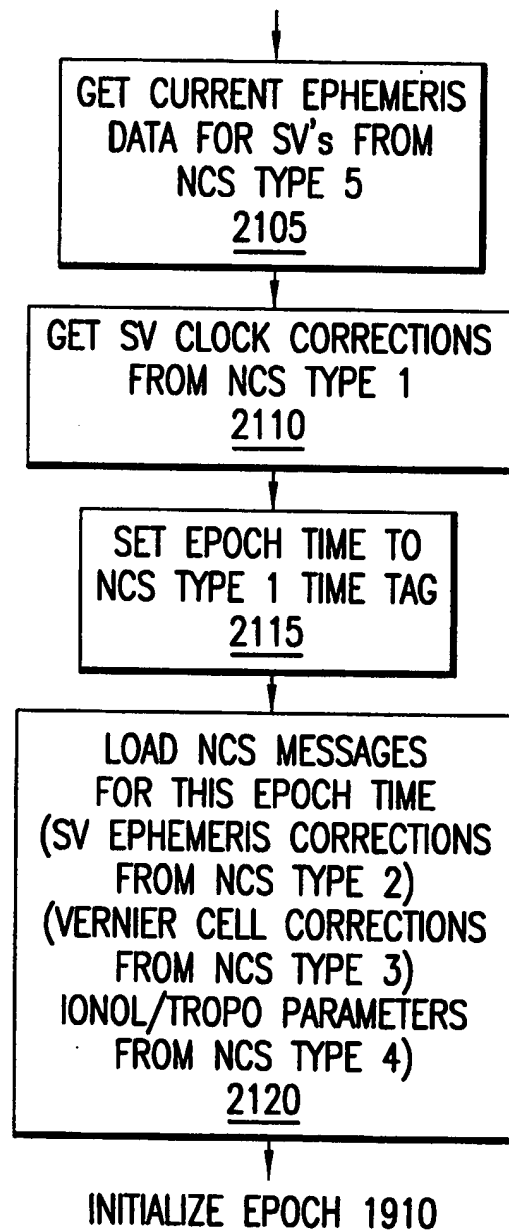
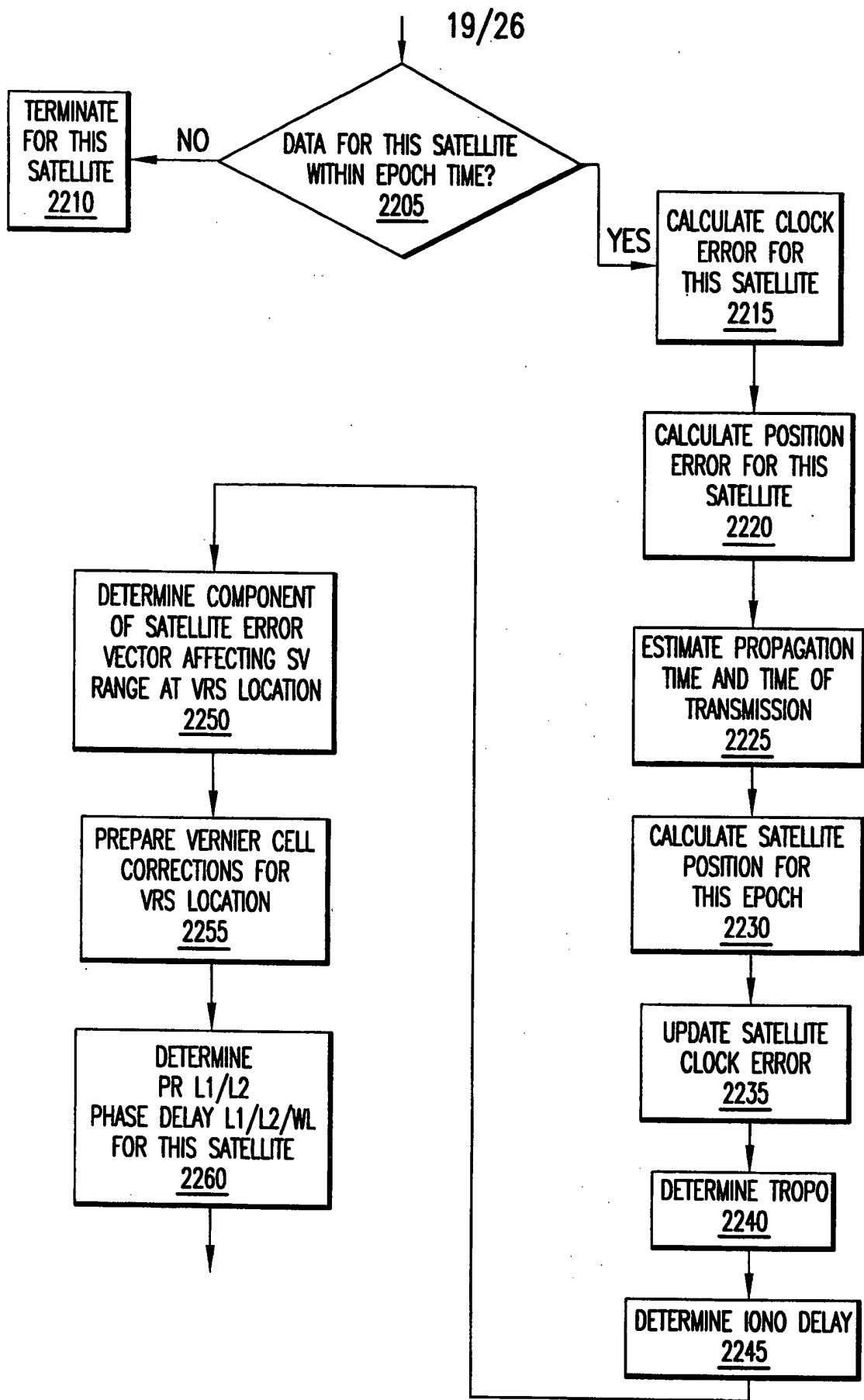
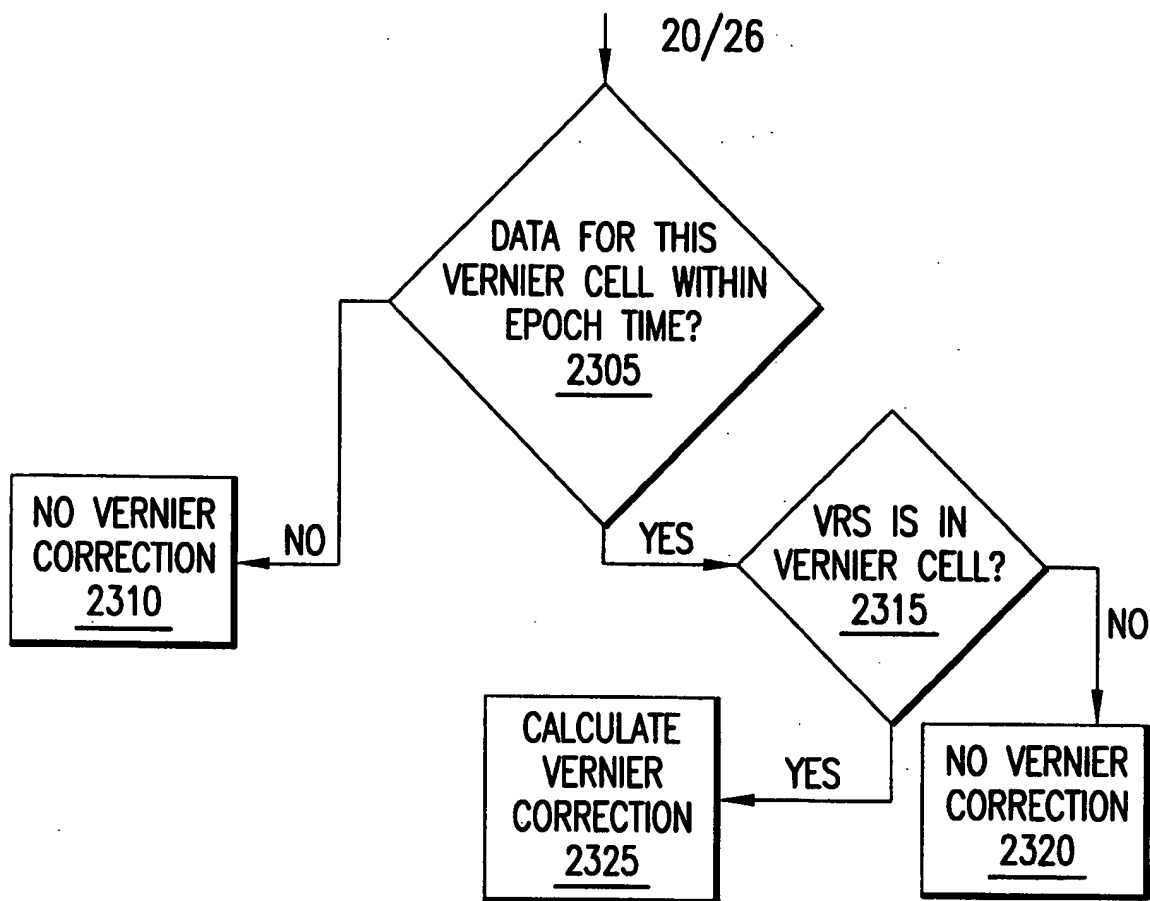


FIG. 21



PROCESS EPOCH 1915

FIG. 22



PREPARE VERNIER CELL CORRECTIONS  
2255

FIG. 23

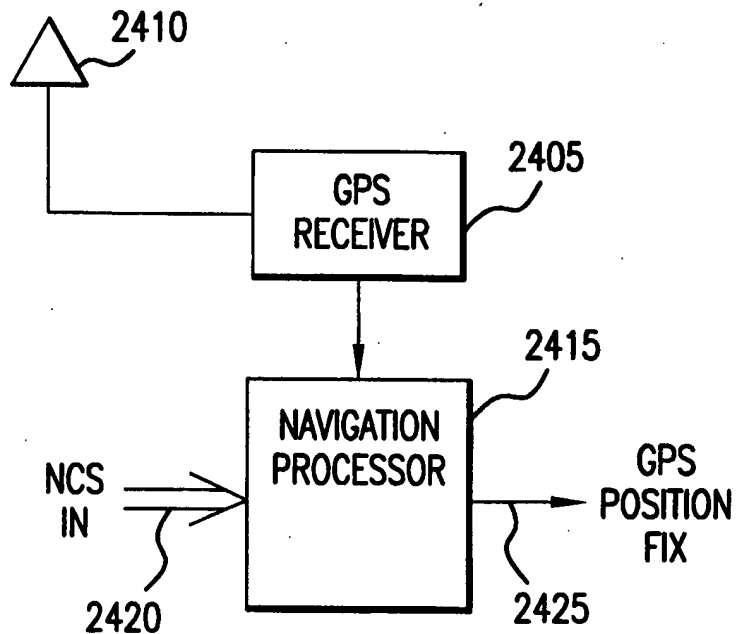


FIG. 24

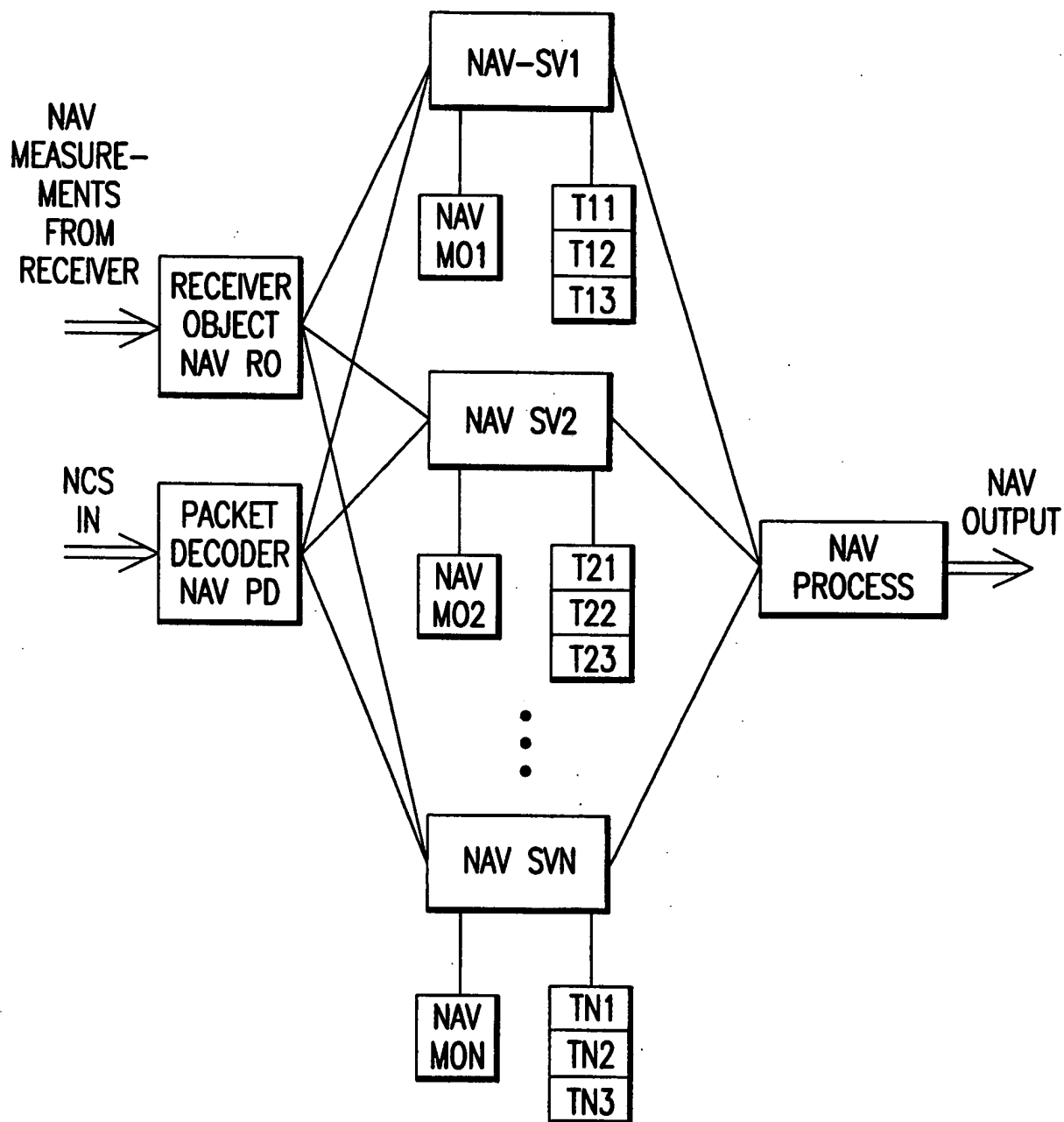
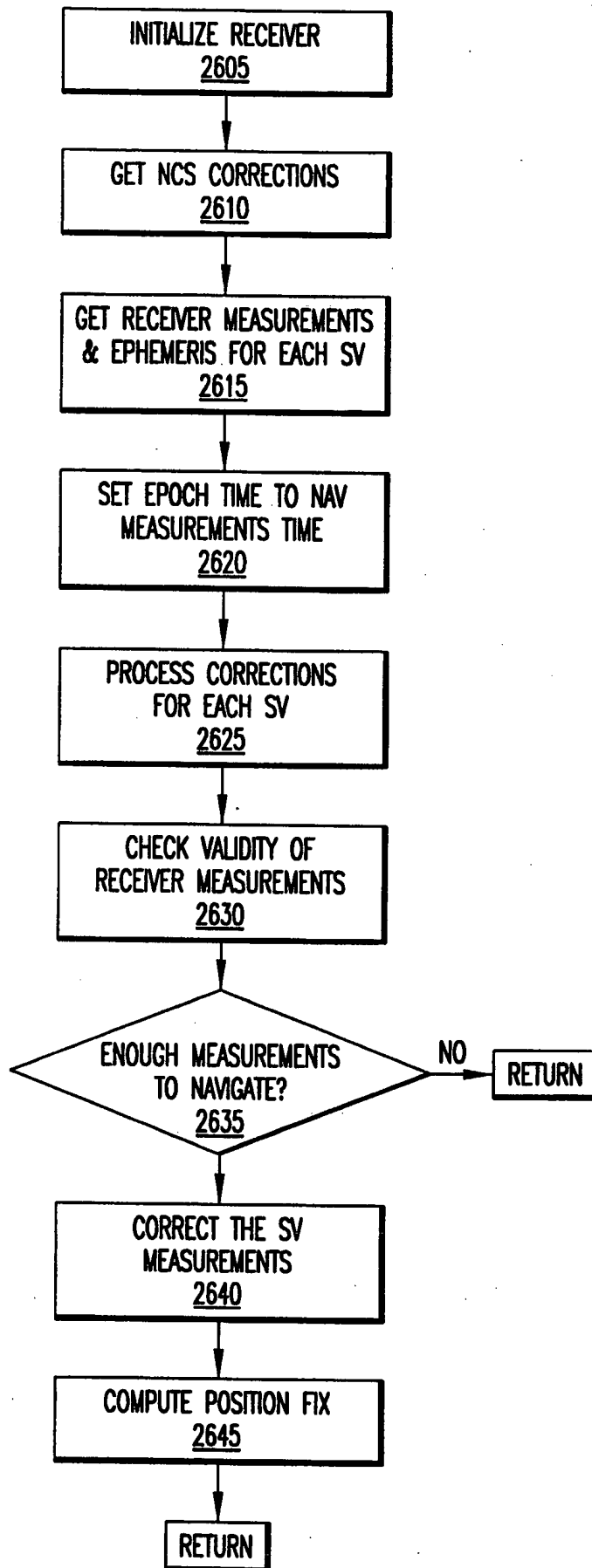
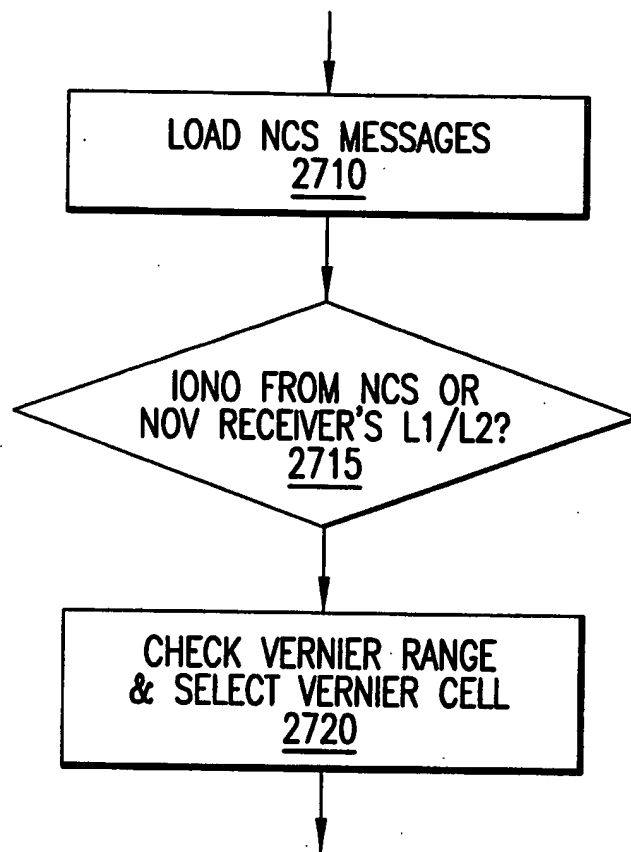


FIG. 25





GET NCS CORRECTIONS 2610

FIG. 27

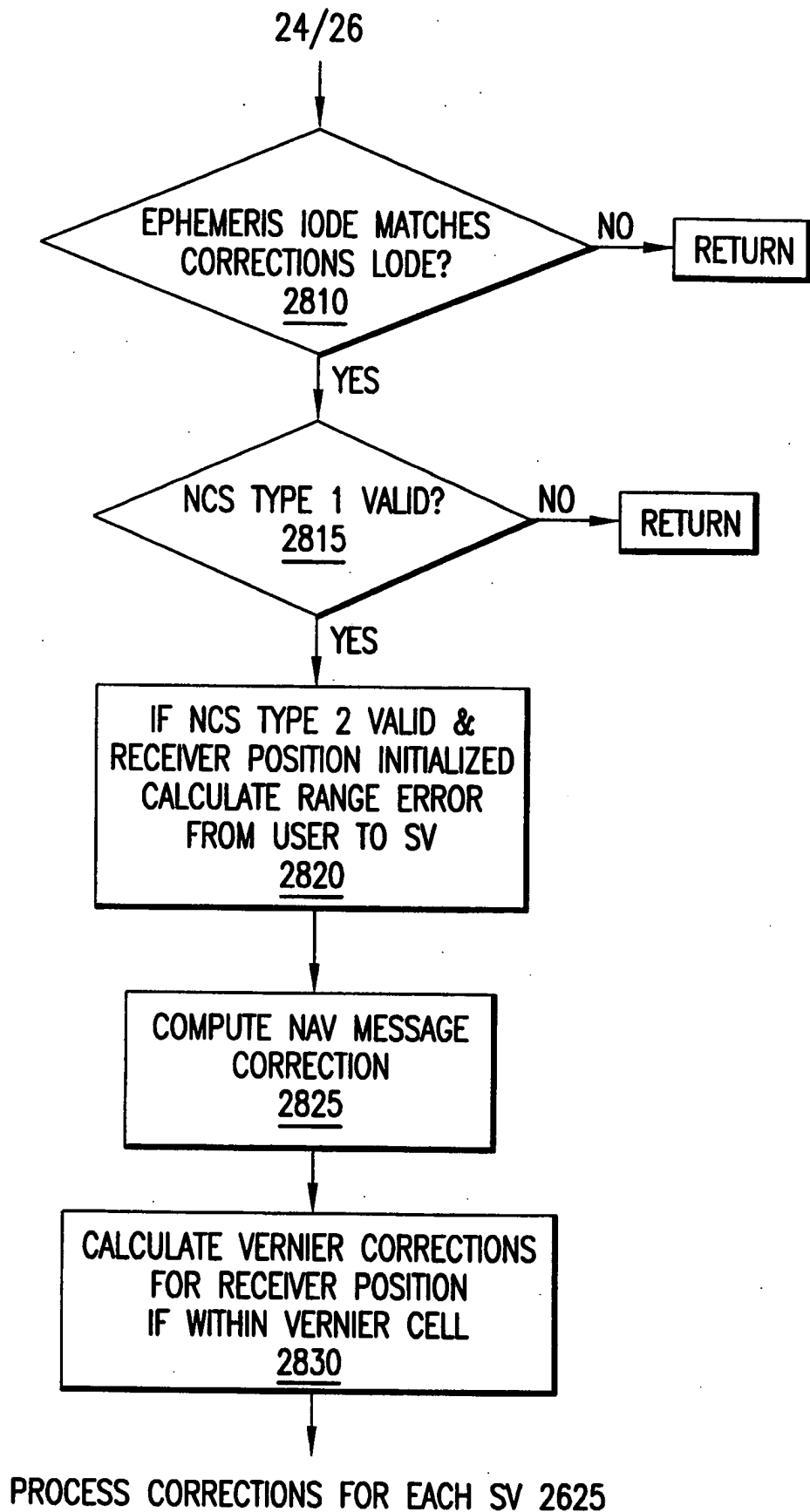


FIG. 28



FIG. 29

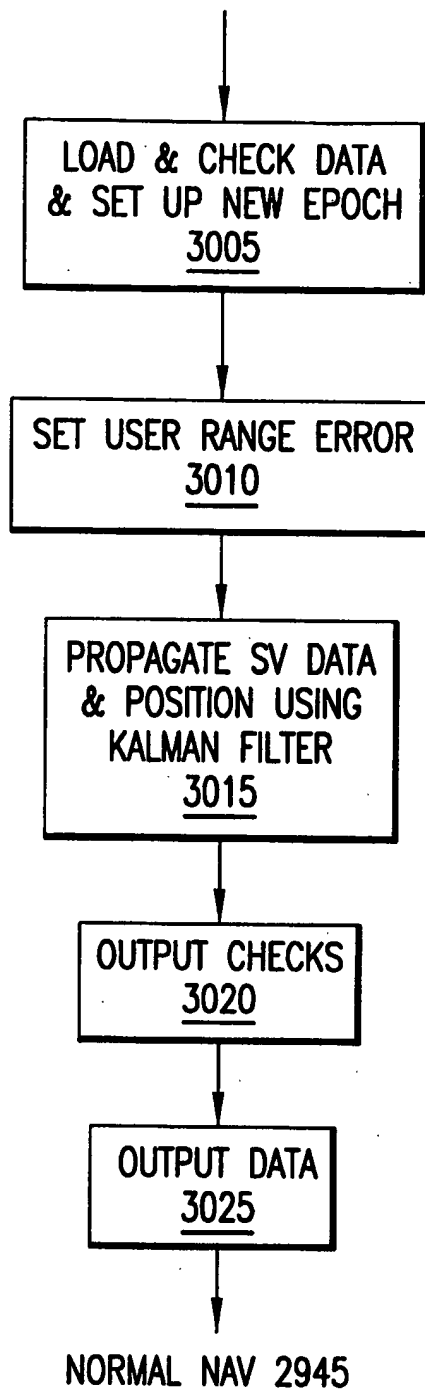


FIG. 30